* Model
  ; Analog M series LCD monitor

- L1510SM
- L1710SM
- L1910SM
- L1515SM
- L1715SM
- L1520BM
- L1720BM
- L1920BM
- L1530SM
- L1730SM
- L1930SM
1. I/F Circuit operation Description
   1) Block diagram
   2) Signal Input block
   3) Supply Voltage regulation block
   4) Scaler Block
   5) Micro controller Block

2. LIPS block operation description
   1) Block diagram
   2) SMPS Block
   3) Inverter Block

3. Appendix
   ; Operation principle of LCD Monitor
1. I/F Circuit operation Description

1.1. Block diagram

- **AC Input**
  - **LIPS**
  - **D-SUB**

- **MST9111A including (ADC/LVDS)**
  - 5V
  - SDA
  - SCL

- **MCU**
  - 5V

- **LCD Module**
  - R,G,B differential
  - LVDS (Low Voltage Differential Signaling)

- **3.3V Reg.**
  - AVDD3.3V
  - DVDD3.3V

- **2.5V Reg.**
  - AVDD2.5V
  - DVDD2.5V

- **AVDD 2.5V**
  - DVDD 2.5V

- **AVDD 3.3V**
  - DVDD 3.3V

- **5V**
  - Reg.
  - AVDD3.3V
  - DVDD3.3V
  - AVDD2.5V
  - DVDD2.5V

- **5V**
  - Reg.
  - AVDD2.5V
  - DVDD2.5V

- **12V**
  - 5V
1. I/F Circuit operation Description

1.2. Signal input Block

This is a signal input circuit diagram.
This block consist of R,G,B, H-sync, V-sync, SCL and SDA signals.

*1) This is a circuit for protection against the ESD.

*2) This is a circuit which is used for impedance matching.
   75 ohm resistors on the R,G,B line are used for impedance matching.

*3) Some Video card output is not stabilized. In this case, unexpected noise may be seen. So this circuit is used for stability of H-sync , V-sync.

*4) ST-DET pin is used to realize the connection of the d-SUB signal cable. This pin is always low (GND) when D-SUB signal cable is connected. In case of disconnection with D-SUB cable, this pin come to be high (5V).

D-SUB PIN Description

<table>
<thead>
<tr>
<th>1: Red</th>
<th>2: Green</th>
</tr>
</thead>
<tbody>
<tr>
<td>3: Blue</td>
<td>4: ID2 (GND)</td>
</tr>
<tr>
<td>5: S.T (GND)</td>
<td>6: GND (Signal RED)</td>
</tr>
<tr>
<td>7: GND (Signal Green)</td>
<td>8: GND (Signal Blue)</td>
</tr>
<tr>
<td>9: 5V</td>
<td>10: GND (Digital)</td>
</tr>
<tr>
<td>11: ID0 (GND)</td>
<td>12: SDA</td>
</tr>
<tr>
<td>13: H - Sync</td>
<td>14: V - Sync</td>
</tr>
<tr>
<td>15: SCL</td>
<td>Sheel : GND</td>
</tr>
</tbody>
</table>
1. I/F Circuit operation Description

1.3. Supply Voltage regulation block

This is a supply voltage regulation block.
This block consist of 3.3V regulator, 2.5V regulator, panel Vcc voltage switching circuit.

*1) This is a voltage regulation circuit for 3.3V output.

*2) This is a voltage regulation circuit for 2.5V output.

*3) This is voltage TR switching circuit which is for panel Vcc power sequence.
   This circuit is used for 15” 17” Model except for 17” AU,19”

*4) This is voltage FET switching circuit which is for panel Vcc power sequence.
   This circuit is used for 17” AU,19” Model.
1. I/F Circuit operation Description

1.4. Scaler block

MST9011B (15”), MST 9111B(17”,19”)

1. Manufacturer : M star
2. Fully integrated ADC, PLL and scaler, LVDS
3. Input sampling rate :
   - MST9011B : 85MHz
   - MST9111B : 135Mhz
4. Input Format :
   - MST9011B : Analog RGB up to XGA (1024 * 768 @75Hz)
   - MST9111B : Analog RGB up to SXGA (1280 * 1024 @75Hz)
5. Output Format : 8 or 6-bit panels
   One (15”) or Two(17”,19”) pixel output format

* Input and output signal

*1) Input block
   - R,G,B input ,
   - H-sync,V-sync,
   - DDC line (D-SDA,D-SCL)

*2) Output block
   - LVDS output (5 channel) including Clock

This Scaler amplifies the level of video signal for the digital conversion and converts from the analog video signal to the digital video signal using a pixel clock and outputs 8-bit R, G, B signal to transmitter.

The pixel clock for each mode is generated by the PLL.

The range of the pixel clock is from 25MHz to 135MHz.
1. I/F Circuit operation Description

1.5. micro-controller block

---

This block consists of u-controller, EEPROM IC which stores control data, and Reset IC

*1) U-controller

The u-controller distinguishes polarity and frequency of the H/V sync are supplied from signal cable. And u-controller control “Inverter on”, “LCD power on”, “Lamp current Adjust” and communication with scaler.

*2) EEPROM

The controlled data of each modes is stored in EEPROM.

*3) Reset block

The reset of the u-controller is active “High” KIA7042 reset IC’s output is low until 5V come to be over 4.2V so that u-controller can have stable reset operation.

---
2. LIPS block operation description

2.1. Block diagram

LIPS Board Block Diagram

- EMI COMPONENTS
- INPUT RECTIFIER AND FILTER
- ENERGY TRANSFER
- OUTPUT RECTIFIER AND FILTER
- PWM CONTROL CIRCUIT
- PHOTO-COUPLER ISOLATION
- SIGNAL COLLECTION
- INVERTER CIRCUIT
- PRIMARY
- SECONDARY

Input: 50 ~ 60Hz, 100 ~ 240V Output: 12V, 5V, GND

High Voltage output

Line connections and signal flow.
2. LIPS block operation description

2.2. SMPS Block
2.2. SMPS Block

This block is SMPS block.

*1) EMI component
   This block construct Low pass filter for.

*2) Input rectifier and smoothing filter
   This block change AC input voltage to high DC voltage

*3) PWM control circuit
   Control PWM oscillator frequency and drive switching MOSFET.

*4) Energy transfer Transformer
   Change high voltage on primary side to low voltage on secondary side and meet the output voltage spec.

*5) Output rectifier and filter
   - Through rectifier diode, get the DC voltage 12V,5V.
   - Construct filter to get more approach DC voltage.

*6) Feedback circuit
   Construct feedback circuit to control U101 wavy duty.
2.3. INVERTER Block
2.3. Inverter Block

This block is Inverter block.

*1) Reset circuit
   This block is for voltage detecting. When input 5V is less than 5VDC,
   U302 KIA7042 will shut down U301(OZ960). U301 (OZ960) will be reset if the voltage is recovered 5VDC.

*2) PWM controller
   U301 (OZ960) is the PWM output controller to drive CCFL.

*3) Drive network
   Dual MOSFET for switch direct network to drive transformer.

*4) Feedback and OVP circuit.
   Detect kick off voltage from transformer and transfer this feedback voltage to pin 2 of U301.
   If the feedback voltage is over 2V, U301(OZ960) will be shut down.
Appendix

Operation principle of LCD Monitor (Analog)

1) LCD Monitor Block diagram
2) Video signal Timing
3) Analog to Digital Converter
4) ADC Calibration
5) Pixel sampling
6) Output TTL Timing
7) LVDS
8) Power sequence for panel
1. LCD Monitor Block diagram

Signal Flow

Analog

Pre-Amp. → A/D Converter → Scaler → LVDS TX

R/G/B → R/G/B → R/G/B 24 bit → R/G/B 24 bit → R/G/B

H/V Sync

Micro-Controller → Clock Generator

Digital

Clock → H Sync

Inverter

H Sync
2. Video signal Timing

2.1. Timing formula

- \( Dclk \ (\text{Mhz}) = H_{total} \times V_{total} \times V_{sync} \) (Refresh Rate)

- \( Dclk = \frac{1}{T_{pixel}} = H_{total} \times H_{sync} \)

- \( H_{sync} = V_{total} \times V_{sync} \)

Vsync = Refresh Rate
Hsync = Horizontal Frequency
Dclk = Pixel clock
2. Video signal Timing

2.2. Timing configuration on Display

H Sync

V Sync

V Start

Active Video Area

H Start

Total Dot = Total Clock

Hsync

Clock
3. Analog to Digital Converter

Pre amp Block

- Amp(0.7:1)
- R/G/B
- Cut off

Analog to Digital Converter Block

- AD Converter
- 8 bit R/G/B data
- 1V=255 : 11111111
- 0V=0 : 00000000

PLL Block

- Hsync
- Loop Filter
- VCO
- ADC Clock
- Divider
4. ADC Calibration

4.1. ADC Calibration Procedure

Each channel of the ADC must be calibrated before it can be used.

1. OFFSET1 is used to remove DC bias offsets in the ADC path.
2. OFFSET2 is used to trim the ADC to the black level characteristics of the RGB source.
3. GAIN is used to align the full scale voltage swing of the external source to the maximum input of the ADC.

OFFSET and GAIN calibration should be done with the real video source source, while capturing a full scale input.
Calibration is performed through firmware routines.
4.2. Offset1 Calibration

* Offset1

  : Compensate for internal DC offset of the input stage of the on-chip track and Hold.

* To compensate the chip to chip variation.

  Therefore, the requirement is to perform only once (at Factory).

* Procedure is:

  - Set video input voltage for 0.0V.
  - set gain to minimum : read ADC outputs
  - Set gain to maximum: read ADC outputs
  - Adjust offset 1 until ADC outputs at minimum and maximum are the same (within +/- tolerance)
4.3. Offset2 Calibration

* Offset2
  : Compensate for internal DC offset of the 2nd stage of the on-chip track and Hold.
* When used with offset1, make the overall ADC offset equal to zero and independent of the ADC gain setting.
* Ideally performed using actual analog input with full range values from graphics source.

• Procedure is:
  – Set video input voltage for 0.0V.
  – Decrease Offset2 to first instance where ADC underflow flags are set
4.4. Gain Calibration

* Gain
  : Used to adjust full range input to produce full –swing ADC codes (from 00h to FFh)
* sometime, called auto color; auto white level; auto balance
* Require a full range input source to be performed correctly

* Procedure is:
  - Set video input voltage for 0.73V (or 0.7V for some model).
  - Increase gain to first instance where ADC overflow flags are set
4.5. Effect of incorrect ADC calibration

* If ADC calibration is performed incorrectly, then following various artifacts might be happened.
  - Saturated “White”
    → different shades close to peak white value can’t be differentiated.
  - “Unblack” black
    → different shades of black close to black floor can’t be differentiated or black doesn’t black enough.
  - Reduced apparent contrast
5. Pixel sampling

5.1. Pixel sampling Point

Input Clock

Input data

Stable Clock/Data Sampling Point
5. Pixel sampling

5.2. How to find best pixel sampling point

* Sum of pixel difference
  : For auto phase adjustment, “sum of pixel difference” method is used.
  The pixel sum is highest at best phase point.

\[ \text{PHASE} = \sum (P_N - P_{N-1}) \]

* To find best phase point is done by firmware routine.
(1) Detail timing description between Clock and Data (Falling Latch)

- **Data Setup** ($T_{\text{SETUP}}$): Data setup time before Falling Edge of Clock.
- **Data Hold** ($T_{\text{HOLD}}$): Data Hold up time after Falling Edge of Clock.
- **DE/Hsync/Vsync Setup** ($T_{\text{SETUP}}$): DE/Hsync/Vsync setup time before Falling Edge of Clock.
- **DE/Hsync/Vsync Hold** ($T_{\text{HOLD}}$): DE/Hsync/Vsync Hold up time after Falling Edge of Clock.

---

### Appendix

6. Output timing
6. Output timing

(2) Output TTL Signal description (measured at Panel side)

① Vertical Front Porch
② Vertical Sync Width
③ Vertical Back Porch
④ Vertical Total : Active Line + Vertical Bank Porch + Vertical Front Porch
⑤ Horizontal Front Porch
⑥ Horizontal Sync Width
⑦ Horizontal Back Porch
⑧ Horizontal Total : Active Pixel + Horizontal Back Porch + Horizontal Front Porch
⑨ Active Line : Active Line Data
⑩ Active Data : Active Pixel Data
7.1. LVDS (Low voltage differential signaling)

Convert TTL signal to Low voltage differential signal.
8. Power sequence for Panel

Notes:
1. Please avoid floating state of interface signal at invalid period.
2. When the interface signal is invalid, be sure to pull down the power supply for LCD Vcc to 0V. Invalid signal with Vcc for a long period of time, causes permanent damage to LCD panel.
3. Lamp power must be turn on after power supply for LCD and interface signals are valid.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td>T 1</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>T 2</td>
<td>0.01</td>
<td>–</td>
</tr>
<tr>
<td>T 3</td>
<td>200</td>
<td>–</td>
</tr>
<tr>
<td>T 4</td>
<td>200</td>
<td>–</td>
</tr>
<tr>
<td>T 5</td>
<td>0.01</td>
<td>–</td>
</tr>
<tr>
<td>T 6</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>T 7</td>
<td>1</td>
<td>–</td>
</tr>
</tbody>
</table>

Appendix