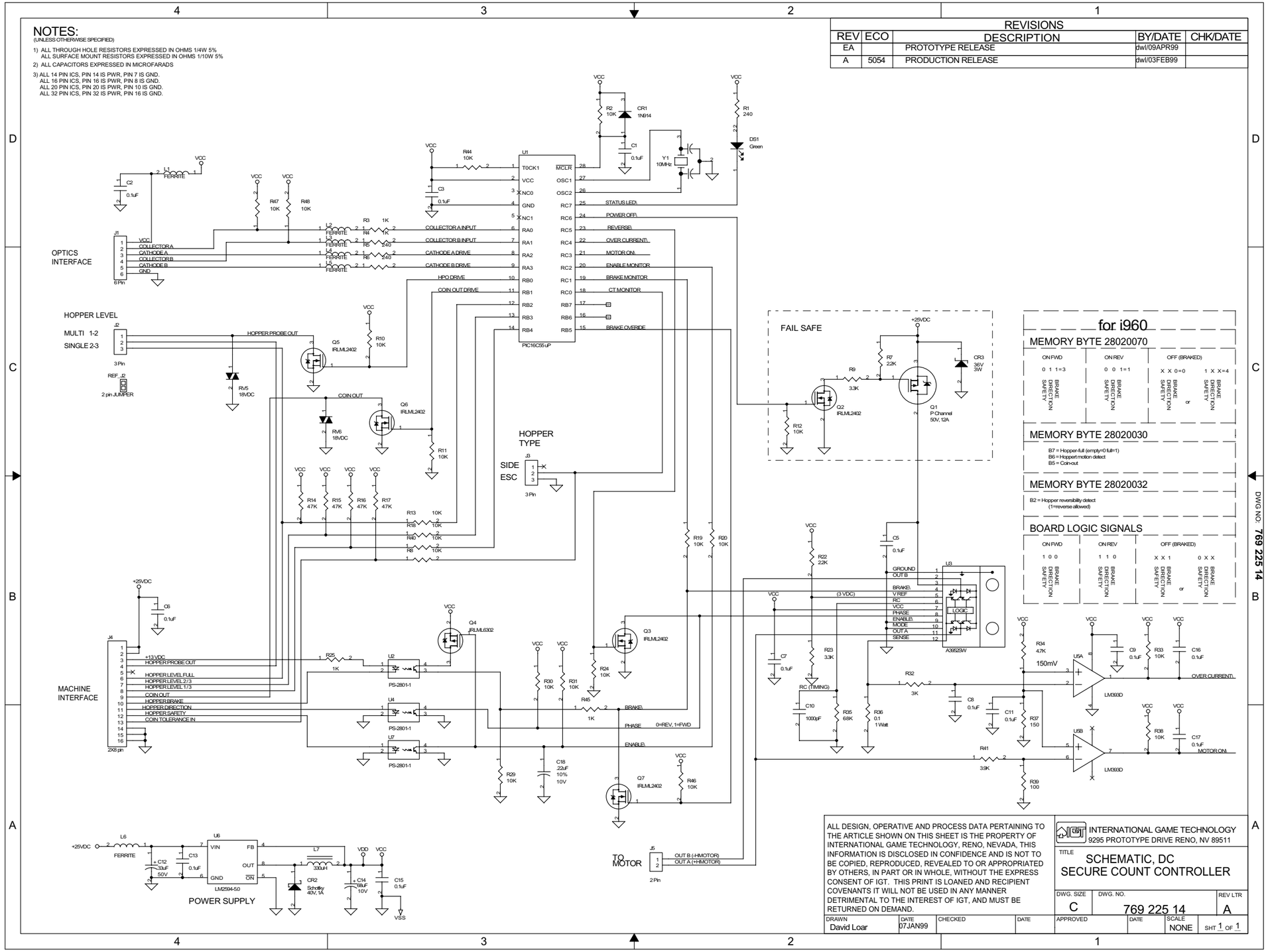
NOTES:
(UNLESS OTHERWISE SPECIFIED)
1) ALL THROUGH HOLE RESISTORS EXPRESSED IN OHMS 1/4W 5%
ALL SURFACE MOUNT RESISTORS EXPRESSED IN OHMS 1/10W 5%
2) ALL CAPACITORS EXPRESSED IN MICROFARADS
3) ALL 14 PIN ICS, PIN 14 IS PWR, PIN 7 IS GND.
ALL 16 PIN ICS, PIN 16 IS PWR, PIN 8 IS GND.
ALL 20 PIN ICS, PIN 20 IS PWR, PIN 10 IS GND.
ALL 32 PIN ICS, PIN 32 IS PWR, PIN 16 IS GND.
REVISIONS
REV ECO DESCRIPTION BY/DATE CHK/DATE
EA PROTOTYPE RELEASE dwl/09APR99
A 5054 PRODUCTION RELEASE dwl/03FEB99
OPTICS INTERFACE
HOPPER LEVEL
MULTI 1-2
SINGLE 2-3
MACHINE INTERFACE
POWER SUPPLY
HOPPER TYPE
SIDE
ESC
TO MOTOR
FAIL SAFE
U1
PIC16C55-uP
U3
A3952SW
LOGIC
U5A
U5B
LM393D
U6
LM2594-50
for i960
MEMORY BYTE 28020070
ON FWD
ON REV
OFF (BRAKED)
MEMORY BYTE 28020030
B7 = Hopper-full (empty=0 full=1)
B6 = Hoppert motion detect
B5 = Coin-out
MEMORY BYTE 28020032
B2 = Hopper reversibility detect
(1=reverse allowed)
BOARD LOGIC SIGNALS
DWG NO: 769 225 14
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INTERNATIONAL GAME TECHNOLOGY
9295 PROTOTYPE DRIVE RENO, NV 89511
TITLE
SCHEMATIC, DC
SECURE COUNT CONTROLLER
DWG. SIZE C
DWG. NO. 769 225 14
REV LTR A
DRAWN David Loar
DATE 07JAN99
CHECKED
DATE
APPROVED
DATE
SCALE NONE
SHT 1 OF 1