TP6720 LCD Monitor Controller

I. General Description

The TP6720 is a single-chip analog panel monitor controller, with easy-to-operate and powerful features, used in flat panel monitor for PC computing system. It contains all the logic required to convert PC VGA signals to color TFT/DSTN LCD signals. In order to simplify the panel monitor system, TP6720 uses 208 pins QFP to integrate Clock Generator (Triple PLL frequency synthesizers), OSD Controller and Power Management Controller to minimize the chip-count or board-space with minimum glue logic. The TP6720 includes Memory Controller (MEMC), OSD Controller (OSDC), Display Mode Detector (DMD), Address Multiplexer (AMUX), Power Management Controller (PMC), PLL Frequency Synthesizers, Flat Panel Controller, RGB Space Converter and adds an MPU Interface to provide system setup and programming operation. With the deeper line FIFO and the multiple levels of display buffers, the TP6720 supports best system performance even in minimum memory configurations. The TP6720 includes a built-in Frame Rate Controller to adjust the input horizontal/vertical sync. polarity and to provide the input/output frame rate control. It also implements a VESA DDC interface to communicate with users through VGA card and PC system. In addition, the TP6720 provides an 8-bit low byte address latch output for the external expansion ROM of 8x51 MPU and supports MPU with direct read/write frame buffer. The memory controller server as a DRAM controller for the frame buffer, which handles DRAM refresh, display panel refresh, frame buffer access by MPU and supply the control signal of SGRAM or SDRAM. The TP6720 supports flat panel display with resolution up to 1024x768 true-color. The TP6720 also provides an approach to keep the horizontal/vertical resolution of the display mode constant and centers the active display area on the panel. The flat panel interface supports Monochrome/Color STN LCD panel, Color TFT LCD panel with direct panel interface to (DD) Dual-panel , Dual-drive for color and monochrome and (SS) Single-panel , Single-drive (supports 8,9,12,15,16,18,24,36-bit data). The TP6720 offers several types of DRAM to perform different memory configurations including 1MB, 2MB, and 4MB of memory size for different applications. The TP6720 supports 256K/1M x 16-bit SDRAM or 256 x 32 bit SGRAM memory to simplify LCD monitors to implement high resolution display. With two of 256K x 16 or

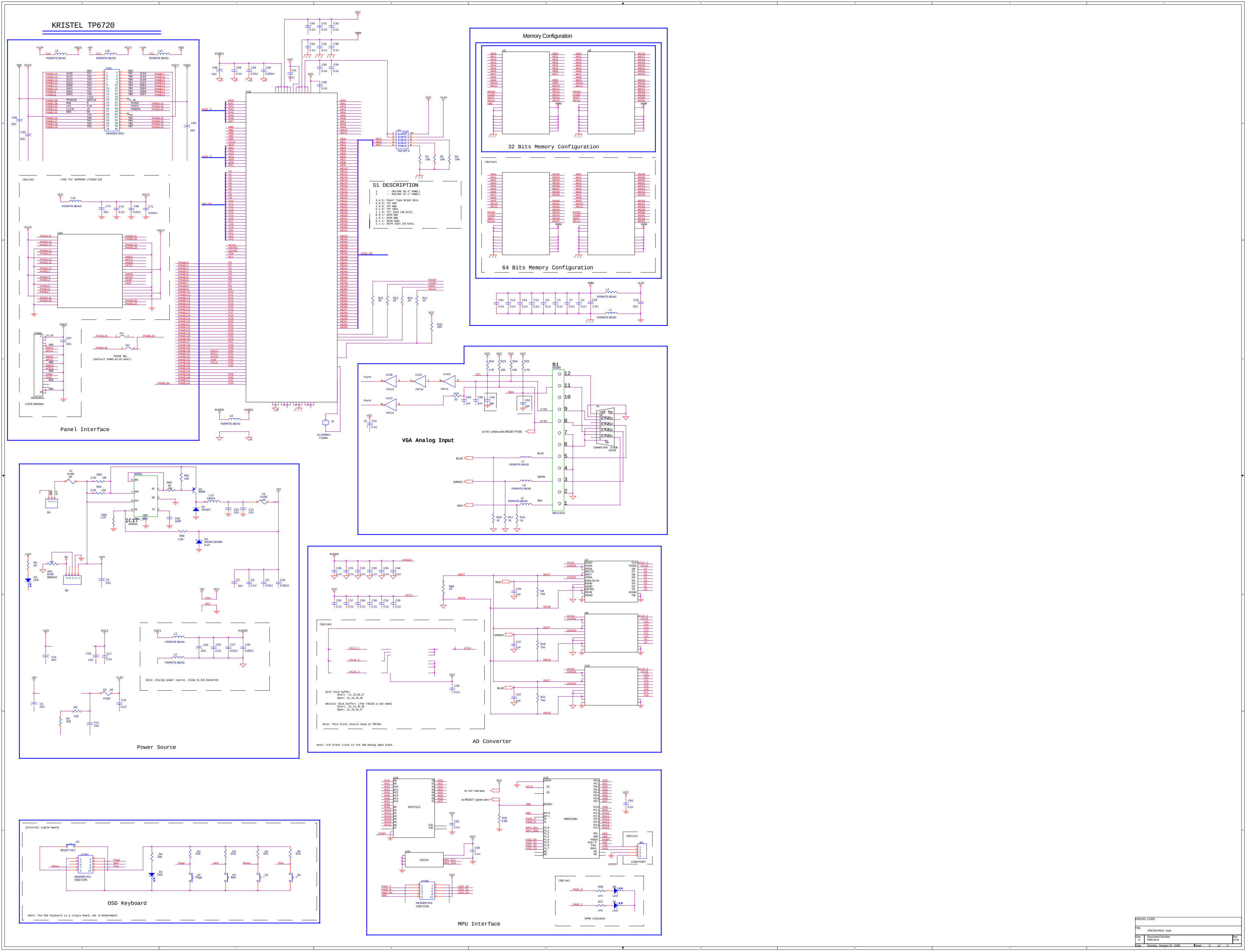
one of 256K x 32, memory size is 1M byte and data width is 32 bits. With four of 256K x 16 or two of 256K x 32, memory size is 2M bytes and data width is 64 bits. With eight of 256K x 16 or four of 256K x 32, memory size is 4M bytes and data width is 64 bits. Specially, with four of 1M x 16, data width is 64 bits and memory size is 8N bytes but the TP6720uses the lower 4M bytes only. Similarly, with two of 1M x 16, data width is 32 bits and the TP6720 uses the lower 2M bytes. The TP6720 also provides the power sequence control for flat panels. FPVCC signal is applied to the digital +5V voltage of flat panel, FPVEE signal is applied to the analog Driver's bias voltage of flat panel, and FPBACK signal is applied to the inverter for the backlight of flat panel. The on/off sequences are programmable. Furthermore, the TP6720 provides intelligent control to switch power mode automatically ("On" for VESA DPMS 'On mode', and "Off" for VESA DPMS power off mode including Off, standby and suspend) to save the power of TP6720 and Panel. The TP6720 has been designed to optimize performance/cost considerations. The VGA clock(VCLK) and Panel clock (PCLK) rate, up to 100MHz, depends upon the mode used. The Memory clock (MCLK) input, up to 100 MHz, is optional and depends on the frame buffer DRAMs access-time.

II. Features

* Provided 3-channel of RGB data input
  - Flexible 24/16/12-bit digital data input selection
* VGA input Sync. capability
  - Horizontal Sync. : 15k ~ 60 KHz
  - Vertical Sync. : 55-90 Hz
  - VGA input maximum pixel rate : 100 MHz
* Support Flat Panel resolution up to 1024x768
* Flat Panel types support
  - Color TFT LCD Panel
  - Color Dual-Scan STN LCD Panel
* Color TFT LCD Panel support
  - Support 36/24-bit 2-pixels/clock data interface
  - Support 24/18-bit 1-pixels/clock data interface
  - Support 16/15/12/9-bit 1-pixels/clock data interface
* Color Dual-Scan STN LCD Panel support
  - Support 24-bit 4-pixels/clock data interface
  - Support 16-bit 8-pixels/3-clocks data interface
* Flat panel function support
  - Amplitude modulation for color TFT LCD Panel
  - Color dithering for Dual-Scan STN LCD Panel
  - Shadow frame buffer interface for Dual-Scan STN LCD Panel

- Pseudo frame buffer technique for Dual-Scan STN LCD Panel
- Panel horizontal/vertical expansion
- Panel horizontal pixel faded

* Flat panel frame buffer DRAM type support
  - Provide SDRAM, and SGRAM memory configuration
  - Support 32-bit or 64-bit data width memory
* Provided 8x51 micro-processor interface
* Provided flexible OSD (On Screen Display) function control
* Time base clock resource support
  - Integrated triple PLL frequency synthesizers
  - Programmable VGA dot clock and up to 100 MHz
  - Programmable Panel dot clock and up to 100 MHz
  - Programmable/External memory clock and up to 100 MHz
  - Provided a MPU clock output from divided Panel clock
  - Provided a VGA dot clock output for external RGB AD converter
  - Provided a synchronized memory clock output for external SDRAM or SGRAM
* VESA DDC interface support
  - Support DDC1 (unidirectional) and DDC2B (bi-directional, I^2C-compatible interface)
* VESA DPMS support
  - Built-In Power Management controller for Green PC of EPA Energy-Star support
  - Support multiple level power down : On/Standby/Suspend/Off mode
  - Delay power on control to protect flat panel
* Automatic VGA display mode detection and switching control
* 208 PQFP Package
* 3/5 volt operation


KRISTEL TP6720
Memory Configuration
32 Bits Memory Configuration
64 Bits Memory Configuration
S1 DESCRIPTION
VGA Analog Input
Panel Interface
Power Source
AD Converter
OSD Keyboard
MPU Interface