U3000 VGA/SVGA
Theory of Operation

SWITCHMODE POWER SUPPLY

AC power is converted to DC by a bridge rectifier consisting of D101, D102, D103 and D104 and by filter capacitor C105. Start up voltage for U101 is supplied through R102 and R103. U101 oscillator frequency is determined by the values of R116 and C116. Pin 6 of U101 provides a square wave output to drive the switching MOSFET Q101. The switching action of Q101 generates a square wave using the primary of T101 as a load. A network consisting of C106, R104 and D107 acts as a snubber to prevent voltage spikes generated during switching from reaching levels that could damage Q101. Power is transferred to the secondary windings through the transformer action of T101. Voltages from the secondary windings are rectified and filtered providing output voltages to supply the monitor.

Voltage regulation is achieved by sensing the output voltage of a tertiary winding on T101. The voltage on this winding is rectified and filtered by D112 and C121 and fed to pin 2 of U101 through a divider network. This sense voltage varies in proportion to the output voltage and is used to change the duty cycle of the square wave drive to Q101 in order to correct changes in the output voltage. The waveform from the tertiary winding is also fed through D113 and C118 to generate the DC supply voltage for U101.

Current foldback is used to protect the supply from excessive load current. The current through Q101 is sensed at R108 and a proportional voltage is fed into pin 3 of U101. If the voltage at pin 3 exceeds 0.6VDC, U101 shuts off the output at pin 6. U101 will periodically try to restart; however if the load fault is still present, the supply will continue to go into the shutdown mode. This condition will cause the supply to produce a slight ticking sound.

SYNC DECODER OPERATION

Vertical sync is fed into a pair of Exclusive Or (XOR) Gates (pins 9 and 12 of U302). This circuit configuration will provide a negative sync output at pin 8 for the vertical processor regardless of the polarity of the input signal. In addition, the output at pin 11 will be at a high or low logic level depending on the polarity of the vertical sync signal. This logic signal is fed to pin 3 of the decoder IC U301.

Horizontal sync is fed into pin 5 of a second pair of XOR gates (pin 2 and pin 5 of U302) and is processed in a manner similar to the vertical sync signal. The negative horizontal sync output is provided at pin 6 and the DC logic signal for the decoder IC is provided at pin 3. In addition, the negative horizontal sync is fed to the frequency sensing circuit consisting of U303A and B.

The frequency sensing circuit detects whether a 31.5khz (VGA) or a 35khz (SVGA) signal is present. Pin 5 is high for a 31.5khz signal (modes 1, 2 and 3) and low for a 35khz signal (mode 4). This logic signal is inverted by Q301 and fed to U301, Q302 and Q303. For VGA modes 1, 2 and 3, decoder IC U301 will pull down pins 4, 5 and 6, selecting R319, R320 or R321 to set the vertical size for the detected mode. For the 35khz SVGA mode, the outputs of U301 remain floating (high) and Q301 turns on, causing the vertical size to be set by VR318. In addition, Q302 turns on which turns on Q706 causing R746 to become part of the horizontal oscillator RC circuit (in parallel with R710 and VR701). This causes the horizontal oscillator frequency to increase to 35khz.

HORIZONTAL CIRCUIT

Horizontal sync from the decoder circuit is applied to pin 1 of U700. The fist section of U700 is an adjustable delay, the delay being determined by the values of C701, R706 and VR700. Adjusting VR700 will move the position of the video on the screen horizontally. The output of the delay circuit is fed to the phase detector which compares the frequency of the sync signal to the frequency of the horizontal oscillator and produces a DC correction voltage to keep the oscillator frequency locked to the incoming sync frequency. The DC correction voltage is fed through R708 to the oscillator. The free running frequency of the oscillator is set by VR701.

HIGH VOLTAGE SHUTDOWN CIRCUIT

The flyback pulse is sensed from the filament winding (pin 9) of the flyback transformer. The pulse is converted to a DC level proportional to the high voltage by D710 and C729. VR702 is adjusted so that when the high voltage exceeds an acceptable level, the internal X-Ray protect circuit of U700 (pin 13) will turn off the horizontal oscillator causing the high voltage to drop to zero. This circuit acts as a latch; therefore power to the monitor must be turned off for a few seconds in order to reset this circuit after it has been tripped.

VIDEO CIRCUIT

Red, green and blue video signals are applied to pins 10, 9 and 8 of P301 and are AC coupled to the video processor IC U200. DC bias for the input amplifiers is provided from the output of pin 11 through R206, R207 and R250. The gain or contrast of the RGB amplifiers is controlled simultaneously by the DC voltage applied at pin 12, which varies with the setting of the contrast control VR201.

DC restoration occurs during retrace when the input signal is at black level. A negative pulse derived from the horizontal sync amplifier Q205 is applied to the clamp gate input at pin 14. During this pulse, the black level of the signal is clamped to a DC level, which is determined by the setting of the brightness control VR200. RGB output signals from U200 are fed through buffer amplifiers Q200, Q201 and Q202 to the neck board cascode video amplifiers. The outputs of these amplifiers are fed to the CRT cathodes.

Pulling down the video signals to below black level during the horizontal and vertical-blanking periods provides blanking. This is accomplished by turning on Q204 (vertical) or Q208 (horizontal), turning on diodes D209, D210 and D211, forcing the video outputs low. The horizontal blanking signal is derived from the filament pulse, and the vertical blanking signal is derived from the vertical retrace pulse.

Sensing the voltage developed across R801 provides beam limiting. When beam current reaches approximately 800uA, Q800 begins to turn on and Q801 begins to turn off. AS Q801 turns off, the voltage applied to the CRT grid 1 begins to go negative, causing the beam current to limit.

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